

# CLC001

## Serial Digital Cable Driver with Adjustable Outputs

### General Description

The CLC001 is a monolithic, high-speed cable driver designed for use in SMPTE 259M serial digital video and ITU-T G.703 serial digital data transmission applications. The CLC001 drives 75Ω transmission lines (Belden 8281 or equivalent) at data rates up to 622 Mbps. Controlled output rise and fall times (400 ps typical) minimize transition-induced jitter. The output voltage swing is adjustable from 800 mV<sub>p-p</sub> to 1.0 V<sub>p-p</sub> using an external resistor.

The CLC001's output stage consumes less power than other designs. The differential inputs accept LVDS signal levels, LVPECL levels directly or PECL with attenuation networks.

All these make the CLC001 an excellent general purpose high speed driver for high-speed, long distance data transmission applications.

The CLC001 is powered from a single +3.3V supply and comes in a small 8-pin SOIC package.

### Key Specifications

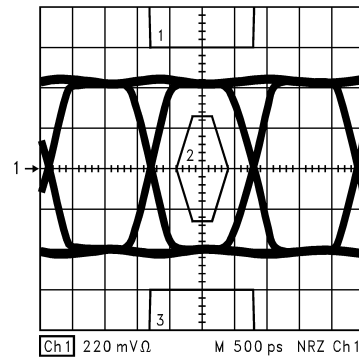
- 400 ps rise and fall times
- Data rates to 622 Mbps
- 100 mV differential input threshold
- Low residual jitter

### Features

- Adjustable output amplitude
- Differential input and output
- Accepts LVPECL or LVDS input swings
- Low power dissipation
- Single +3.3V supply

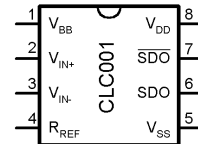
### Applications

- Digital routers and distribution amplifiers
- Coaxial cable driver for digital transmission lines
- Twisted pair driver
- Serial digital video interfaces for the commercial and broadcast industry
- SMPTE, Sonet/SDH, and ATM compatible driver
- Buffer applications



622 Mbps Eye Pattern with STM-4 Signal Mask

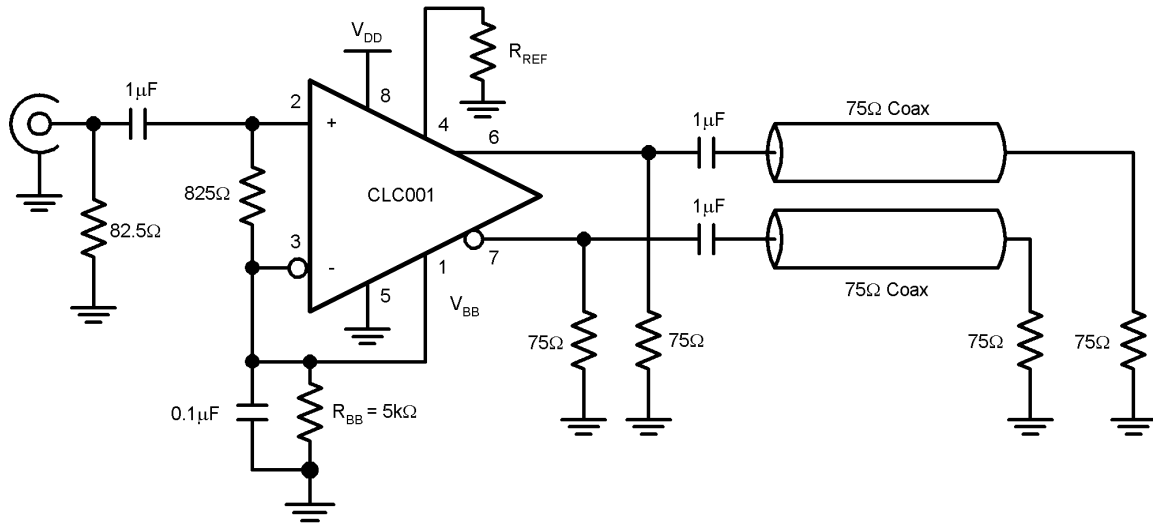
### Connection Diagram (8-Pin SOIC)



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Order Number CLC001AJE  
See NS Package Number M08A

## Typical Application



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**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	4V
Output Current	27 mA
Maximum Junction Temperature	+125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 seconds)	+300°C
ESD Rating (HBM)	≥ 7 kV
ESD Rating (MM)	≥ 500V
Package Thermal Resistance $\theta_{JA}$ Surface Mount AJE	125°C/W

 $\theta_{JC}$  Surface Mount AJE

105°C/W

Reliability Information

Transistor count

291

**Recommended Operating Conditions**

Supply Voltage Range ( $V_{DD} - V_{SS}$ )	+3.0V to +3.6V
Operating Free Air Temperature ( $T_A$ )	-40°C to +85°C
$R_{BB}$ Range (applied to $V_{BB}$ input) (Note 6)	1.3k $\Omega$ to 11.5k $\Omega$

**Electrical Characteristics**

Over recommended operating supply and temperature ranges unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OUTPUT DC SPECIFICATIONS</b>						
$V_{SDO}$	Serial Driver Output Voltage	$R_L = 75\Omega$ 1%, $R_{REF} = 1.91$ k $\Omega$ 1% (for 800 mV <sub>p-p</sub> ), Figure 1	720	800	880	mV
		$R_L = 75\Omega$ 1%, $R_{REF} = 1.5$ k $\Omega$ 1% (for 1.0 V <sub>p-p</sub> ), Figure 1	900	1000	1100	mV
<b>INPUT DC SPECIFICATIONS</b>						
$V_{TH}$	Differential Input High Threshold	$V_{CM} = +0.05V$ or +1.2V or +3.25V,		0	+100	mV
$V_{TL}$	Differential Input Low Threshold	$V_{DD} = 3.3V$	-100	0		mV
$V_{CMR}$	Common Mode Voltage Range	$V_{ID} = 100mV$ , $V_{DD} = 3.3V$	0.05		3.25	V
$I_{IN}$	Input Current	$V_{IN} = 0V$ or +3.0V, $V_{DD} = 3.6V$ or 0V		±1	±10	$\mu A$
$I_{INB}$	Input Current Balance	$V_{IN} = 0V$ or +3.0V, $V_{DD} = 3.6V$ or 0V, (Note 8)		0.23		$\mu A$
<b>SUPPLY CURRENT</b>						
$I_{DD}$	Total Dynamic Power Supply Current (includes load current)	$R_L = 75\Omega$ , $R_{REF} = 1.91$ k $\Omega$ 1% ( $V_{SDO} = 800$ mV <sub>p-p</sub> @ 270 Mbps)		70	115	mA
		$R_L = 75\Omega$ , $R_{REF} = 1.5$ k $\Omega$ 1% ( $V_{SDO} = 1.0$ V <sub>p-p</sub> @ 622 Mbps)		85	130	mA
<b>MISCELLANEOUS PARAMETERS</b>						
$L_{GEN}$	Output Inductance			6		nH
$R_{GEN}$	Output Resistance			25		k $\Omega$
$I_{BB}$	$V_{BB}$ Current	$R_{REF} = 1.91$ k $\Omega$ 1%, (Note 6)		250		$\mu A$
		$R_{REF} = 1.5$ k $\Omega$ 1%, (Note 6)		315		$\mu A$

## AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_r, t_f$	Rise time, Fall time	20%–80%, (Notes 4, 5)		400	800	ps
$t_{os}$	Output overshoot			5		%
$t_{jit}$	Output jitter	(Note 7)		25		ps
$t_{pd}$	Propagation delay	(Note 5)		1.9		ns

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

**Note 2:** Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to  $V_{SS} = 0V$ .

**Note 3:** Typical values are at 25°C and 3.3V.

**Note 4:** This parameter is Guaranteed by Design.

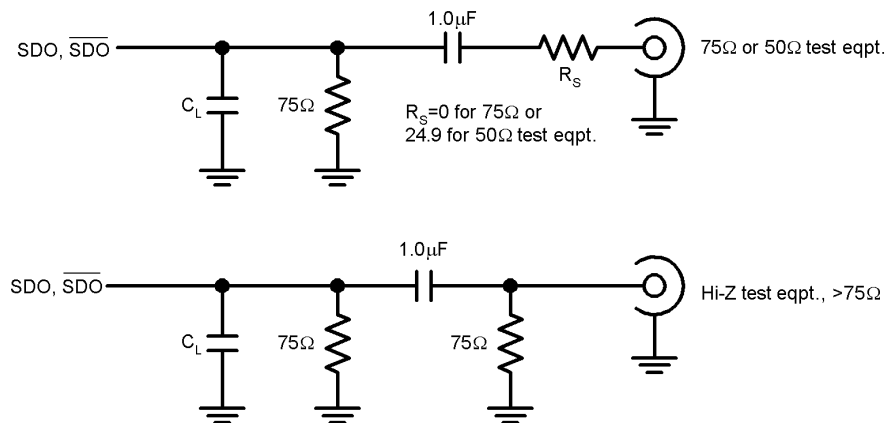
**Note 5:**  $R_L = 75\Omega$ , AC-coupled at 270 Mbps,  $R_{REF} = 1.91\text{ k}\Omega$  1% (for  $V_{SDO} = 800\text{ mV}_{p-p} \pm 10\%$ ),  $C_L$  not greater than 5pF (See Figure 1)

**Note 6:** The  $V_{BB}$  output is intended as a bias supply pin for the inputs of this device only. It is not designed as a power supply output and should not be used to power other devices.

**Note 7:**  $R_L = 75\Omega$ , AC-coupled at 622 Mbps,  $R_{REF} = 1.5\text{ k}\Omega$  1% (for  $V_{SDO} = 1.0\text{ V}_{p-p} \pm 10\%$ ), clock pattern input.

**Note 8:** Input Current Balance ( $I_{INB}$ ) is the difference between the Input Current ( $I_{IN}$ ) on  $V_{IN+}$  and  $V_{IN-}$  for the same bias condition.

## Test Loads



$C_L$  represents probe and test fixture capacitance and is not greater than 5pF.

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FIGURE 1. Test Loads

## Test Loads (Continued)

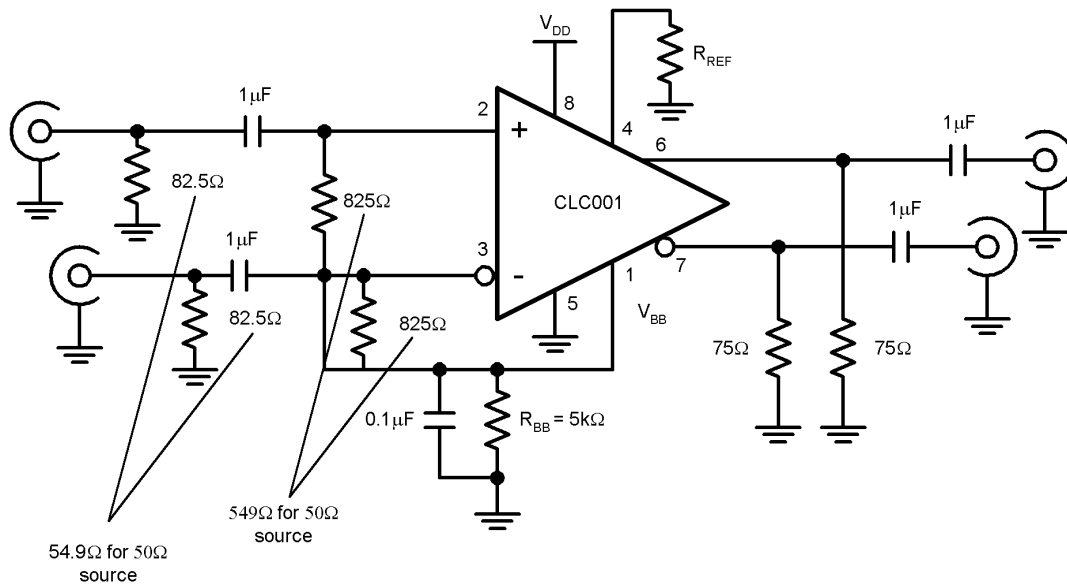


FIGURE 2. Test Circuit

## Pin Descriptions

Pin #	Name	Description
1	$V_{BB}$	Optional, bias voltage (may be used to bias inputs) - see device operation section for details. If unused leave as no connect (NC).
2	$V_{IN+}$	Positive input pin
3	$V_{IN-}$	Negative input pin
4	$R_{REF}$	Output driver level control. Connect a resistor to ground to set output voltage swing.
5	$V_{SS}$	Negative power supply
6	SDO	Serial data true output
7	$\overline{SDO}$	Serial data complement output
8	$V_{DD}$	Positive power supply

## Device Operation

### INPUT INTERFACING

Numerous input configurations exist for applying PECL, LVPECL, and LVDS signals to the input of the CLC001. Inputs may be single-ended or differential, AC or DC coupled.

The  $V_{BB}$  pin may be used to provide a DC bias voltage to the inputs. Leave this pin as a no connect when no bias is needed. Note that DC-coupled inputs such as direct LVDS and LVPECL connections are self-biasing and do not require use of the  $V_{BB}$  pin.  $I_{BB}$ , the current produced by the  $V_{BB}$  pin, depends on  $R_{REF}$ . For a given  $R_{REF}$ , the  $I_{BB}$  current will remain constant, and the bias voltage is determined by the value of resistance,  $R_{BB}$ , between the  $V_{BB}$  pin and ground. *Figure 3* and *Figure 4* show how  $R_{BB}$  corresponds to some common  $V_{BB}$  values with  $R_{REF}$  held at 1.91 k $\Omega$  and 1.5 k $\Omega$ , respectively. Some common input configurations are shown in *Figure 5* through *Figure 9*.

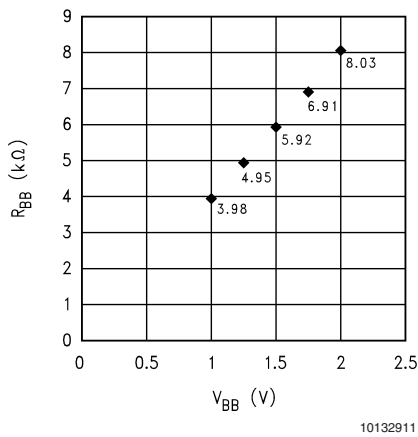


FIGURE 3.  $R_{BB}$  vs.  $V_{BB}$  for  $R_{REF} = 1.91$  k $\Omega$

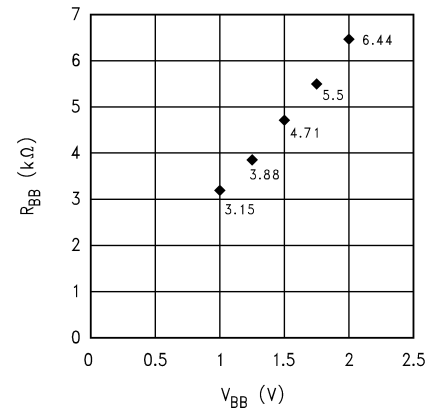
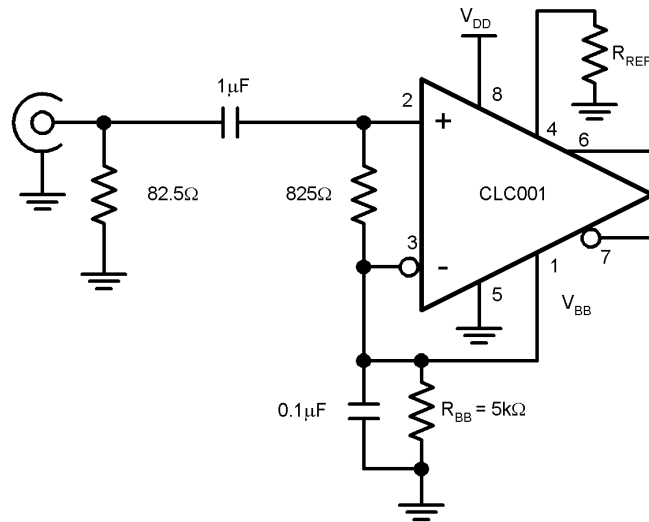


FIGURE 4.  $R_{BB}$  vs.  $V_{BB}$  for  $R_{REF} = 1.5$  k $\Omega$

## Device Operation (Continued)

Figure 5 shows the CLC001 with an AC-coupled, single ended input connection. The  $82.5\Omega$  resistor in parallel with

$825\Omega$  gives the equivalent termination resistance of  $75\Omega$ .  $R_{BB}$  set at  $5k\Omega$  provides  $1.25V$  of DC bias to the input.

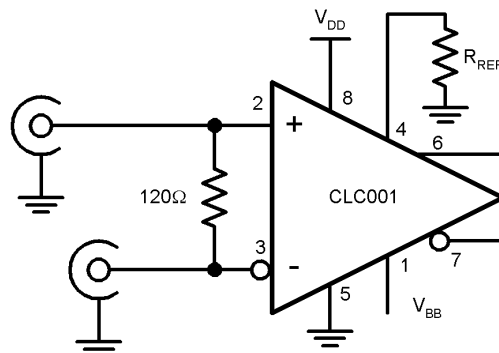


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**FIGURE 5. Single Ended  $75\Omega$  Coaxial Cable, AC-coupled**

A typical DC-coupled, twisted pair cable connection is shown in Figure 6. The CLC001 is driven differentially. The line is terminated with a termination resistor equal to the impedance of the line being driven. The actual resistor value is

media specific, but typically is between  $100$  and  $120\Omega$  depending upon the cable. This resistor should be located close to the CLC001 inputs pins to minimize the resulting stub length between the resistor and device pads.



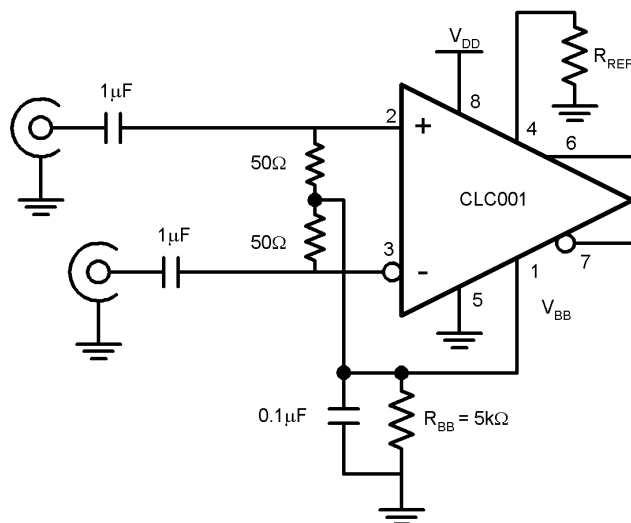
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**FIGURE 6. Twisted Pair Cable, DC-coupled**

## Device Operation (Continued)

Figure 7 shows an AC-coupled, twisted pair cable application. It implements a center tap capacitance termination

used in conjunction with two  $50\Omega$  resistors to filter common mode noise.  $R_{BB}$  set at  $5k\Omega$  provides  $1.25V$  of DC bias to each input.

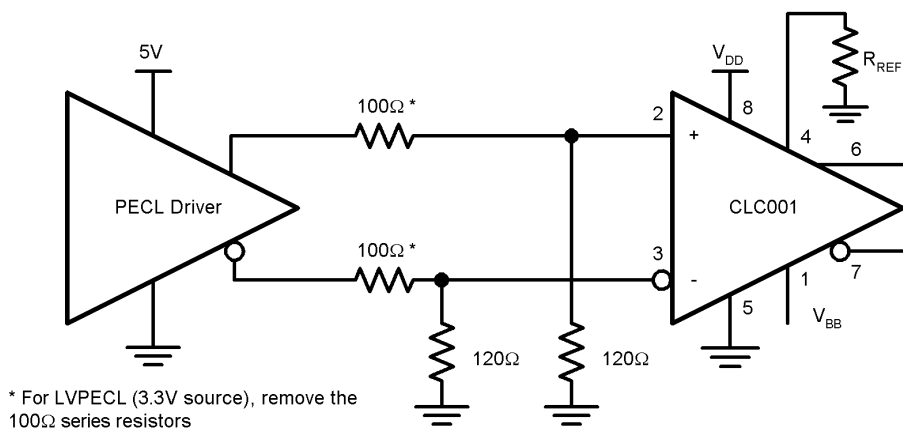


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FIGURE 7. Twisted Pair Cable, AC-coupled

PECL or LVPECL drivers may be interfaced to the CLC001 as shown in Figure 8. The voltage divider network will reduce the PECL output to the proper levels. For LVPECL, the  $100\Omega$  series resistors should be removed, since the common

mode range inputs of the CLC001 are wide enough to accept LVPECL levels directly. No external DC biasing is required for PECL/LVPECL connections.



\* For LVPECL (3.3V source), remove the  $100\Omega$  series resistors

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FIGURE 8. PECL, DC-coupled



## Device Operation (Continued)

A typical LVDS input connection is shown in *Figure 9*. The media is driven differentially by an LVDS driver. The line is terminated with a termination resistor equal to the impedance of the line being driven. The actual resistor value is

media specific, but typically is between 100 and 120 $\Omega$ . This resistor should be located close to the CLC001 inputs pins to minimize the resulting stub length between the resistor and device pads. The CLC001 supports  $\pm 100\text{mV}$  thresholds across the entire LVDS common mode range of 0.1V to 2.3V for a 200mV differential signal.

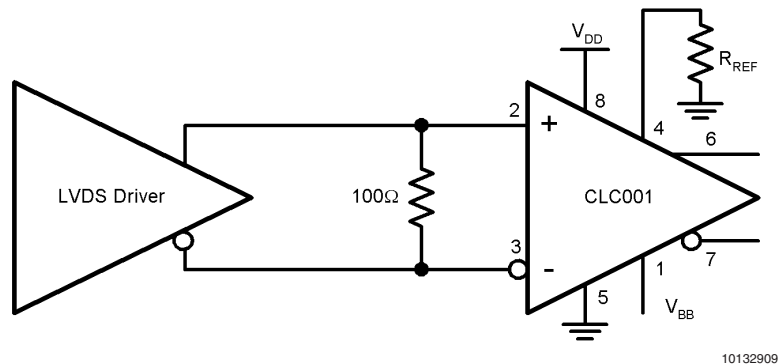


FIGURE 9. LVDS, DC-coupled

## Device Operation (Continued)

### OUTPUT INTERFACING

The CLC001 has two complementary, ground referenced outputs designed to drive AC-coupled and terminated 75Ω coaxial cables. The outputs are single ended; however, they could be treated as a single differential output as long as current paths from each output go to ground.

The output of the CLC001 is a high impedance current source. It expects to see a 75Ω shunt resistor before driving cable to convert the current output to a voltage and provide proper back-matching. No series back-matching resistors should be used. Refer to *Section Typical Application* for an illustration.

Output levels range from 800 mV<sub>p-p</sub> to 1.0 V<sub>p-p</sub> ±10% into 75Ω AC-coupled, back-matched loads. Output level is controlled by the value of R<sub>REF</sub> connected to pin 4. R<sub>REF</sub> is 1.91 kΩ ±1% for 800 mV<sub>p-p</sub>, and 1.5 kΩ ±1% for 1.0 V<sub>p-p</sub>. Refer to *Figure 10* for the output level's sensitivity to R<sub>REF</sub>.

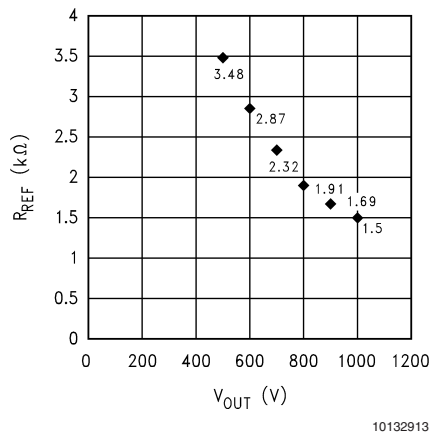


FIGURE 10. Output level's sensitivity to R<sub>REF</sub>

### Evaluation Board

Evaluation boards are available for a nominal charge that demonstrate the basic operation of the SDI/SDV/SDH de-

VICES. The evaluation boards can be ordered through National's Distributors. Supplies are limited, please check for current availability.

The SD001EVK evaluation kit for the CLC001, Serial Digital Cable Driver with Adjustable Outputs, provides an operating environment in which the cable driver can be evaluated by system / hardware designers. The evaluation board has all the needed circuitry and connectors for easy connection and checkout of the device circuit options as discussed in the CLC001 datasheet. A schematic, parts list and pictorial drawing are provided with the board.

From the WWW, the following information may be viewed / downloaded for most evaluation boards: [www.national.com/appinfo/interface](http://www.national.com/appinfo/interface)

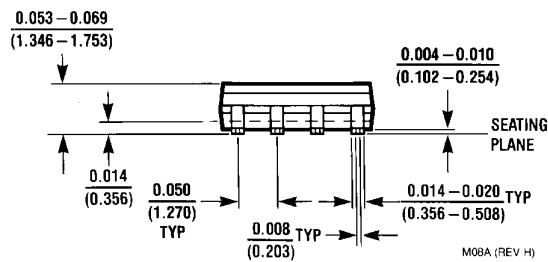
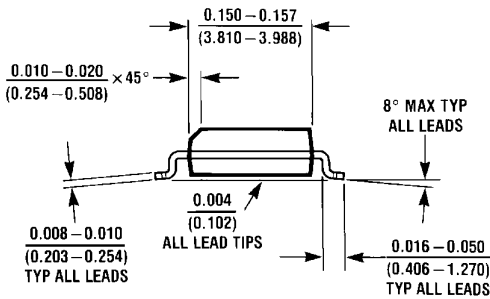
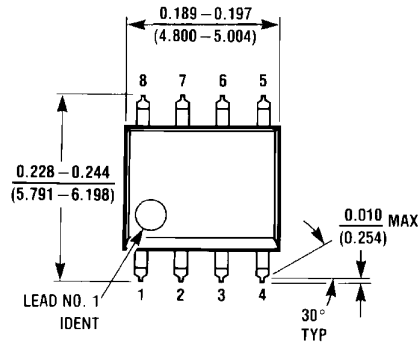
- Device Datasheet and / or EVK User Manual
- View a picture of the EVK
- View the EVK Schematic
- View the top assembly drawing and BOM
- View the bottom assembly drawing and BOM

### PCB Layout Recommendations

Printed circuit board layout affects the performance of the CLC001. The following guidelines will aid in achieving satisfactory device performance.

- Use a ground plane or power/ground plane sandwich design for optimum performance.
- Bypass device power with a 0.01 μF monolithic ceramic capacitor in parallel with a 6.8 μF tantalum electrolytic capacitor located no more than 0.1" (2.5 mm) from the device power pins.
- Provide short, symmetrical ground return paths for:
  - inputs,
  - supply bypass capacitors and
  - the output load.
- Provide short, grounded guard traces located
  - under the centerline of the package,
  - 0.1" (2.5 mm) from the package pins
  - on both top and bottom of the board with connecting vias.

**Physical Dimensions** inches (millimeters) unless otherwise noted



Order Number CLC001AJE  
NS Package Number M08A

M08A (REV H)

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